REMARKS

Claims 1-8 are pending in the Application.

Claims 1, and 3-8 stand rejected.

Claim 2 stands objected to.

I. OBJECTION TO THE SPECIFICATION

Claims 1, 7 and 8 have been objected to because FIR should be replaced by finite impulse response. Claims 1, 7 and 8 have been amended to rewrite the first instance of FIR filter as a finite impulse response (FIR) filter.

II. REJECTION UNDER 35 U.S.C. § 103

Claims 1 and 3-8 have been rejected under 35 U.S.C. §103 as being obvious over *Cabler et al.*, U.S. Patent No. 5,656,621 ("the *Cabler* reference") in view of "Signal Processing Toolbox for Use with Matlab," Chapter 5, pages 5-1 through 5-23 (the "*Matlab*" reference). The Applicants respectfully traverse the rejection of claims 1-8 under 35 U.S.C. §103.

Claim 1 is directed to an integrated circuit. The integrated circuit of claim 1 includes an analog-to-digital converter, a FIR filter, and an output mechanism providing either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data. The Examiner asserts that *Cabler* discloses an integrated circuit including an analog-to-digital converter (**900**) and a FIR filter (**902**). The Examiner admits that *Cabler* does not disclose an output mechanism selectively providing either only fully settled data from the FIR filter or all data from the FIR filter. (Paper No. 10,

page 2.) The Examiner contends that the *Matlab* reference discloses a signal browser that selectively provides a partial/fully settled result by editing the time axis or a full result from the FIR filter by clicking the full view button on the tool bar. (Paper No. 10, page 3.) Plainly the *Matlab* reference does not disclose an output mechanism providing either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data.

The *Matlab* reference is a User's Guide for the Signal Processing Toolbox for use with Matlab® software. (*Matlab*, page 1.) Matlab® is a software platform that provides a set of tools for implementing an environment for technical computing applications. The Signal Processing Toolbox includes a graphical user interface (GUI) called SPTool. (*Matlab*, page 5-2.) the signal Browser relied upon by the Examiner is a component of SPTool that provides a graphical view of signal objects currently selected in SPTool. (*Matlab*, page 5-2.) The GUIs use a set of controls for viewing signals. (*Matlab*, page 5-30.) Zoom-in and zoom-out controls change the scales on the display axes. (*Matlab*, page 5-31.) The full view control restores the displayed signal to its full sample size in both axes. (*Id.*) These controls have nothing to do with the signal being displayed. The signal is not affected by the display controls. This feature is no different than resizing a window in a word processing application. Changing the size of the page does not alter the contents or formatting of the document, but only its appearance on the screen. In particular, changing the scale of the displayed signal does not affect whether the signal includes only fully settled data from a FIR filter or all the data from a FIR filter. Indeed, the signal displayed is not necessarily the output of a FIR filter at all.

Thus, neither the Cabler reference nor the Matlab reference teach or suggest all of the limitations of claim 1. Moreover, a *prima facie* showing of obviousness requires that there be a reasonable expectation of success in combining the references to make

the claimed invention. MPEP § 2143. Evidence of a reasonable expectation of success must be found in the prior art. *Id.* The Examiner has provided no evidence of such a reasonable expectation of success, and there is no expectation of success to make the claimed invention by engrafting a GUI for displaying signals with variable axis scales into the device of the *Cabler* reference.

Lastly, a *prima facie* showing of obviousness requires that there be some motivation or suggestion found in the references themselves, the nature of the problem to be solved or the knowledge of persons of ordinary skill in the art to combine the references. MPEP § 2143.01.

Thus, the teaching relied upon by the Examiner does not disclose an output mechanism selectively providing either a partial result or a full result from a FIR filter, as the Examiner contends.

The Examiner also asserts that it would have been obvious to one of ordinary skill in the art to add an output mechanism selector into Figure 2 of the *Cabler* reference for selecting the desired results to the FIR filter as seen in the *Matlab* reference into Figure 1 because it would enable the operator to select the portion of the desired signals, to reduce the initial unsteady state, and to increase the immunity from process variation. However, as noted above, the *Matlab* reference has not been shown to teach either an output mechanism for selectively providing a full or partial result from the FIR filter. Moreover, the asserted motivation to modify the teachings of *Cabler* do not address the limitations of claim 1. Claim 1 does not recite mechanisms for selecting the portion of the desired results of a FIR filter. Moreover, the alleged motivation of selecting the portion of the desired signals, to reduce the initial unsteady state, etc., are not found in one of the three sources of such a motivation. (*See* MPEP §2143.01.)

Furthermore, these statements are not clear and particular ones of a motivation or suggestion to combine references, but broad conclusory statements regarding the teachings of the reference itself. Such broad conclusory statements are not evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1616 (Fed. Cir. 1999).

Therefore, for at least the aforesaid reasons, the Applicants respectfully assert that a *prima facie* showing of obviousness has not been made with respect to claim 1. Consequently, claim 1 is allowable under 35 U.S.C. §103 over the *Cabler* reference and the *Matlab* reference. M.P.E.P. §2143.

Claim 3 is directed to the integrated circuit of claim 1 in which the output mechanism comprises one or more bits on a register of the integrated circuit to which a user can set to control the selection of fully settled data from the FIR filter or all data from the FIR filter, including unsettled data. The Examiner contends the *Matlab* reference teaches a window "of output the filtered data wherein the output data can be selectively output by editing the axis parameters of the edit boxes." (Paper No. 10, page 3.) The Examiner also states that the edit boxes are manipulated to select only a portion of the data. (Paper No. 10, page 3.) However, the *Matlab* reference does not state the use of the edit boxes. (*Matlab*, page 5-23.) That notwithstanding, the *Matlab* reference does not teach an output of a FIR filter that is either fully-settled data or all the data. Indeed, the display need not be an output signal of a FIR filter at all. The Examiner further contends that the parameters must be stored in a register. (Paper No. 10, page 3.) Because no teaching in the *Matlab* reference refers to registers, the Applicants understand that the Examiner's assertion is tantamount to an allegation that the registers are inherent. However, inherency requires that the Examiner establish that

the registers necessarily be present in the thing described in the reference and it would be so recognized by persons of ordinary skill in the art. MPEP § 2112. This cannot be done because there is no reason that the values in the edit boxes are stored in a register. They could be stored in main memory, or depending on the idiosyncrasies of the operating system on which the particular Matlab® software is running and its segment loading algorithms, on the disk drive. In any case, the *Matlab* reference does not save these values in a register that is included in an output mechanism as recited in claim 3. Thus, the Examiner has not shown that the *Cabler* and *Matlab* references, alone or in combination, teach or suggest all of the limitations of claim 3.

The Examiner states the same motivation for combining the *Cabler* and *Matlab* references to make the invention of claim 3 as stated in conjunction with claim 1, namely, to increase performance for selectively outputting the desired portion of filter data. This motivation is defective for the same reason as the motivation asserted with respect to claim 1. Therefore, the Applicants respectfully contend that a *prima facie* showing of obviousness has not been made with respect to claim 3, and claim 3 is allowable over the *Cabler* and *Matlab* references.

The rejection of claims 4-8 repeat the rejections in the previous Office Action, Paper No. 7.

Claim 4 further depends from claim 3 and recites the integrated circuit thereof in which the one or more bits on a register of the integrated circuit are set over a serial port interface. The Examiner contends that the limitation of claim 4 is taught by *Cabler* in disclosing serial EEPROM **570**. (Paper No. 10, page 4.) As an initial matter, the Applicants note that a serial EEPROM is not a serial port. A serial EEPROM is a memory device. Additionally, the *Cabler* reference teaches that serial EEPROM **570** is

used by the CODEC to make the CODEC Plug-and-Play compatible with industry standard buses. (The *Cabler* reference, column 36, lines 10-13.) Serial EEPROM **570** is external to the circuitry taught in the *Cabler* reference and operates in conjunction with external CD-ROM interface **568**. (The *Cabler* reference, column 36, lines 13-20.) Thus, the *Cabler* reference has not been shown to teach or suggest all of the limitations of claim 4. Neither has a motivation or suggestion for modifying the *Cabler* reference to make the invention of claim 4 been provided. Therefore, the Applicants respectfully assert that a *prima facie* showing of obviousness has not been made with respect to claim 4, and claim 4 is therefore allowable under 35 U.S.C. §103 over the *Cabler* reference.

Claim 5 is directed to the integrated circuit of claim 1 in which the analog-to-digital converter is a delta-sigma modulator. Although the Applicants do not dispute that the *Cabler* reference teaches a delta-sigma modulator ADC, claim 5 is not directed to a delta sigma modulator ADC standing alone. For the reasons discussed hereinabove, the *Cabler* reference has not been shown to teach a delta-sigma ADC in an integrated circuit including the ADC, a FIR filter, and an output mechanism selectively providing either only fully settled data from the FIR or all the data from the FIR including unsettled data. Therefore, the *Cabler* reference has not been shown to teach or suggest all of the limitations of claim 5. Neither has a motivation or suggestion for modifying the *Cabler* reference to make the invention of claim 5 been provided. Thus, the Applicants respectfully assert that a *prima facie* showing of obviousness has not been made with respect to claim 5, and claim 5 is allowable under 35 U.S.C. §103 over the *Cabler* reference.

Claim 6 depends from claim 1 and recites the integrated circuit thereof in which the FIR filter is a decimation filter. Again, the Applicants do not dispute that *Cabler*

teaches a FIR decimation filter. However, again, the *Cabler* reference has not been shown to teach or suggest a FIR decimation filter as recited in claim 6, which includes the limitations of claim 1 from which it depends. Consequently, for at least these reasons, a *prima facie* showing of obviousness has not been made with respect to claim 6, and claim 6 is allowable over the *Cabler* reference.

Claim 7 is directed to a method of designing an integrated circuit having a FIR filter. The method includes the step of providing a mechanism to permit a user to select either only fully settled data from the FIR filter or all data from the FIR filter, including unsettled data. Claim 7 has been rejected on the same rationale as claim 1. (Paper No. 7, page 5.) For at least the reasons discussed hereinabove in conjunction with claim 1, the Applicants respectfully contend that the *Cabler* reference has not been shown to teach or suggest a method of designing an integrated circuit having a FIR filter including a step of providing a mechanism to permit the user to select either or only fully settled data from the FIR filter or all data from the FIR filter. As previously discussed, the Examiner has identified no teaching in the *Cabler* reference whatsoever directed to selecting data from a FIR filter. Thus, because, for at least the reasons that the *Cabler* has not been shown to teach or suggest all of the limitations of claim 7, nor has there been provided a motivation or suggestion for modifying the *Cabler* reference to make the invention of claim 7 sufficient to sustain a *prima facie* showing of obviousness, the Applicants respectfully assert that claim 7 is allowable under 35 U.S.C. §103 over the *Cabler* reference.

Claim 8 is directed to a method of fabricating an integrated circuit having a FIR filter, the method includes the step of providing a mechanism to permit a user to select either only fully settled data from the FIR filter or all data from the FIR filter. Claim 8 has also been rejected on the same rationale as claim 1. (Paper No. 7, page 5.; Paper No

10, page 4.) The Applicants also respectfully contend that claim 8 is allowable under 35 U.S.C. §103 over the *Cabler* reference for at least the reasons that the *Cabler* reference has not been shown to teach or suggest a mechanism permitting a user to select either fully settled data or all the data from the FIR filter, as previously discussed.

III. RESPONSE TO ARGUMENTS

With respect to claim 4, the Examiner states that the Applicants argue that the serial EEPROM is a memory device, not a serial port. It is indisputable that a serial EEPROM is a memory device. It is a Electrically Erasable Programmable Read-Only Memory, hence EEPROM. A read-only memory is a memory device. Indeed the Examiner admits it is a memory device. (Paper No. 10, pages 4-5.) The Examiner's assertion that it communicates with filters 514 or 516 through the control logic and bus interface is without evidentiary support in the *Cabler* reference. As discussed in the Applicants' Reply under 37 C.F.R. 1.111 mailed on August 15, 2003 and hereinabove, the *Cabler* reference teaches that Additionally, the *Cabler* reference teaches that serial EEPROM **570** is used by the CODEC to make the CODEC Plug-and-Play compatible with industry standard buses. (The *Cabler* reference, column 36, lines 10-13.) In other words, the EEPROM stores firmware to configure the control logic and external bus interface. It is not a serial port, and the Examiner does not provide evidence to support the allegation that the serial EEROM taught in the *cabler* reference is a serial port.

With respect to the Examiner's response to the Applicants' arguments regarding claims 5 and 6, the Applicants' argument only reflects the fact that a dependent claim incorporates all of the limitations of the claims from which it depends. 37 C.F.R. § 1.75(c).

IV. ALLOWABLE SUBJECT MATTER

Claim 2 has been objected to as being dependent upon a rejected base claim. Claim 2 has been rewritten hereinabove in independent form.

VI. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that the claims as respectively amended or added in the Application, are in condition for allowance, and Applicants respectfully request an early allowance of such claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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Date: 30 Jan 04